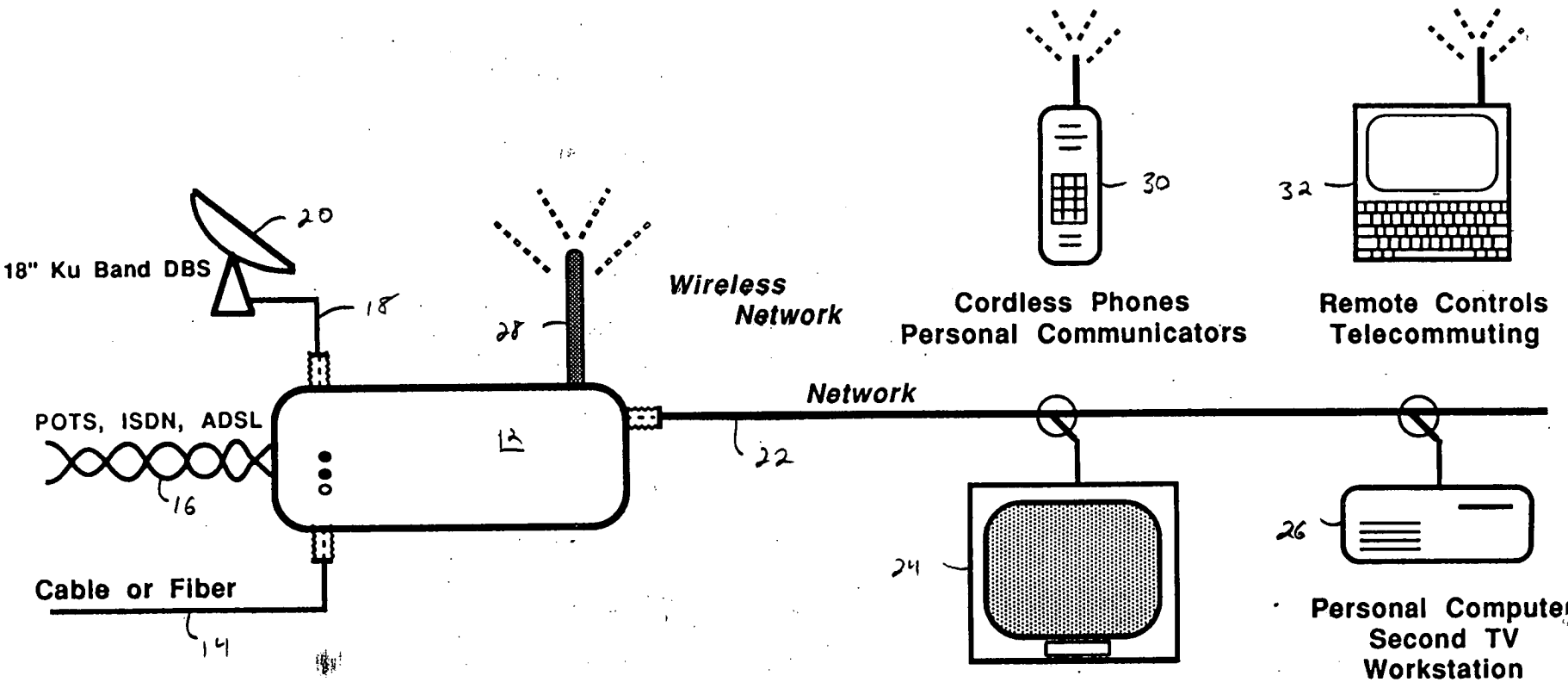

10

Figure 1

08/754827

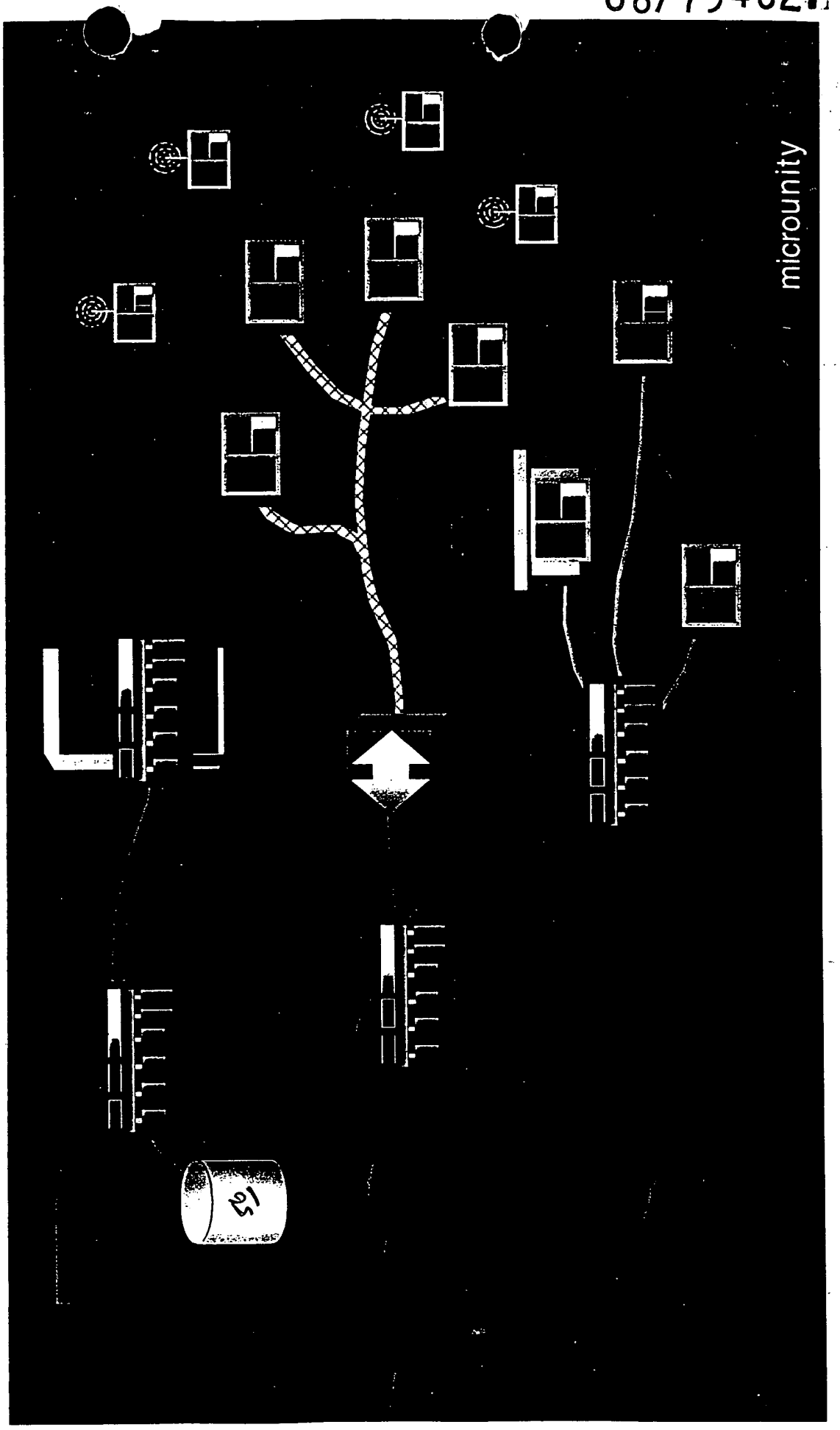

Figure 2

Figure3

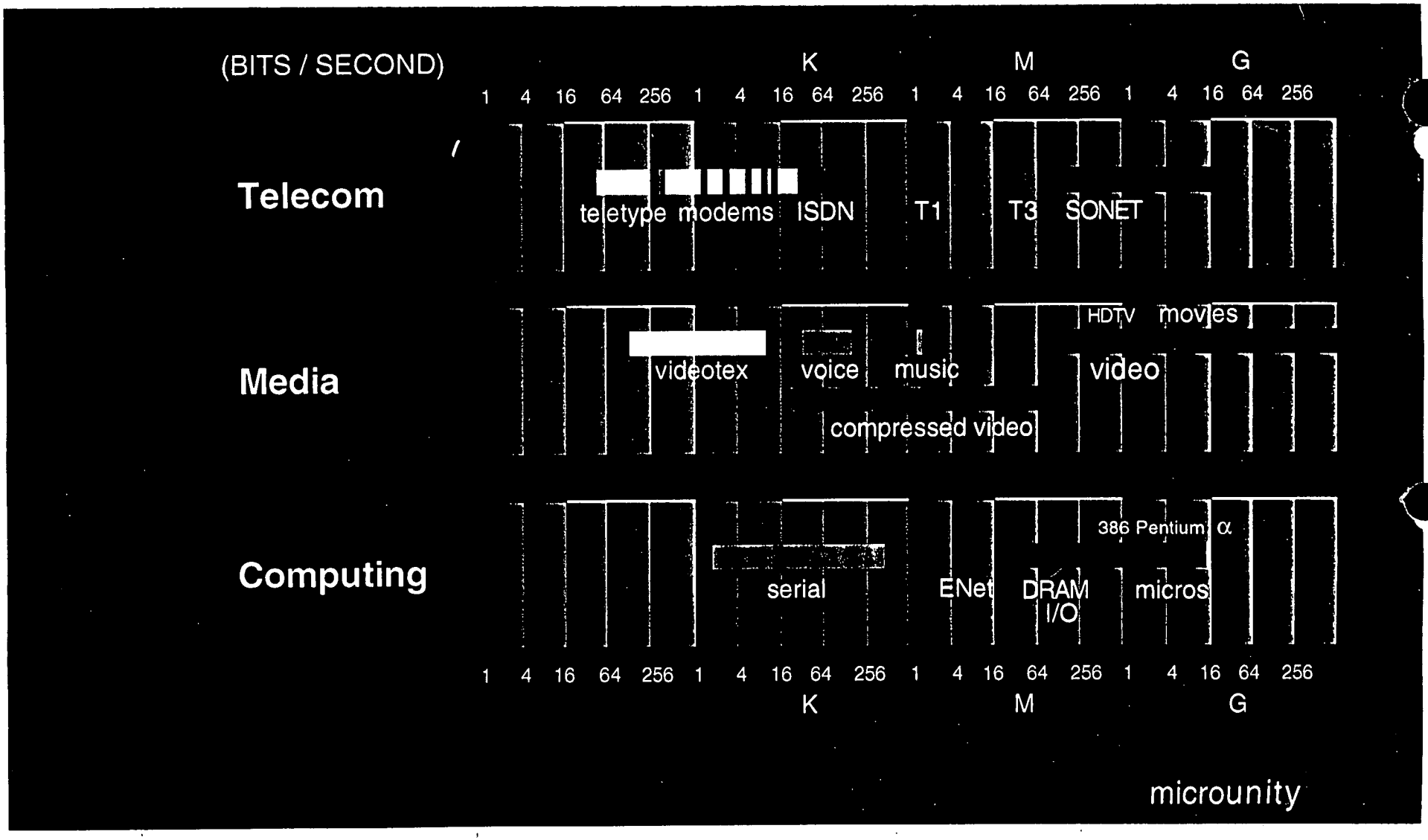

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Figure 4

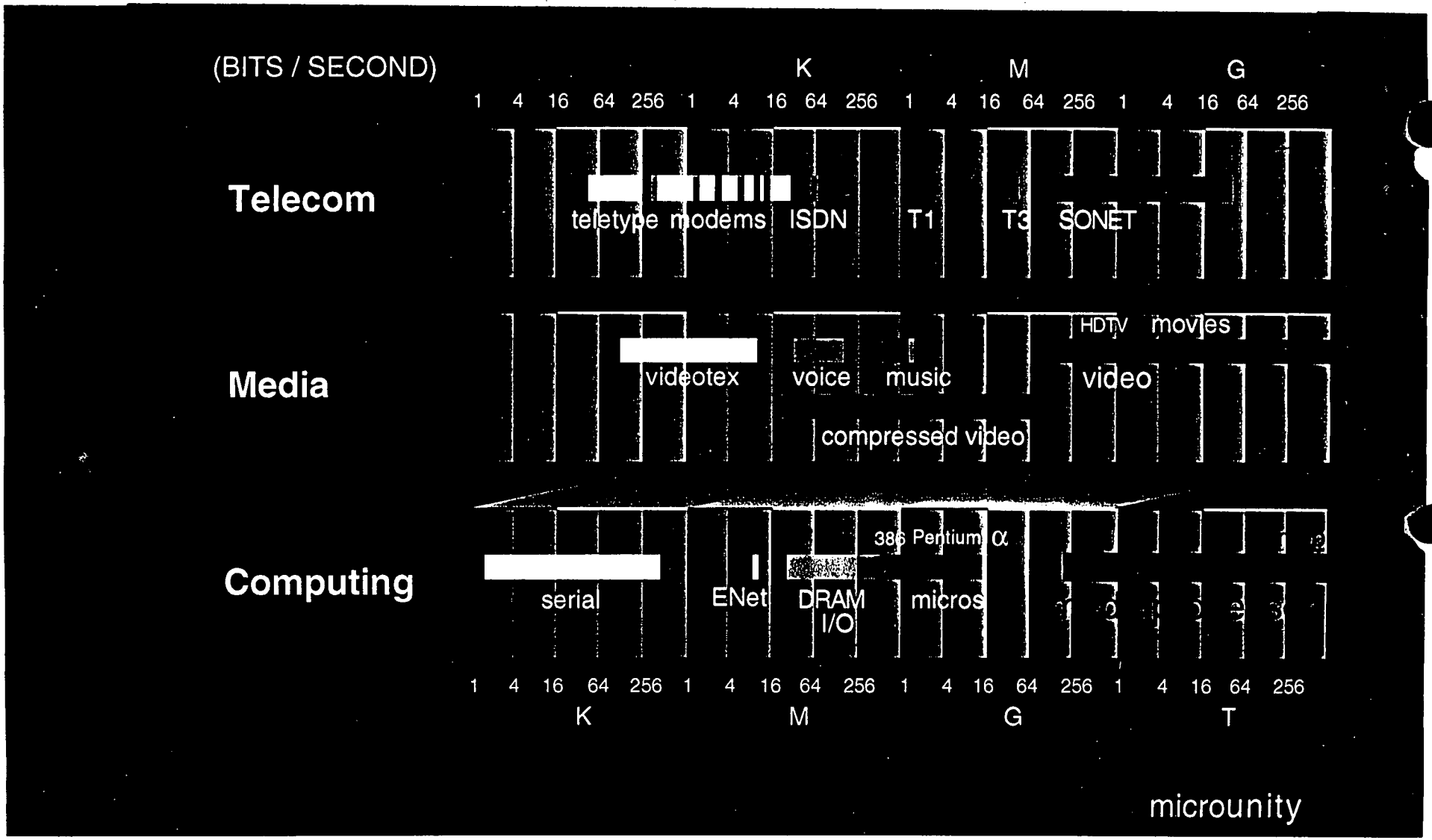

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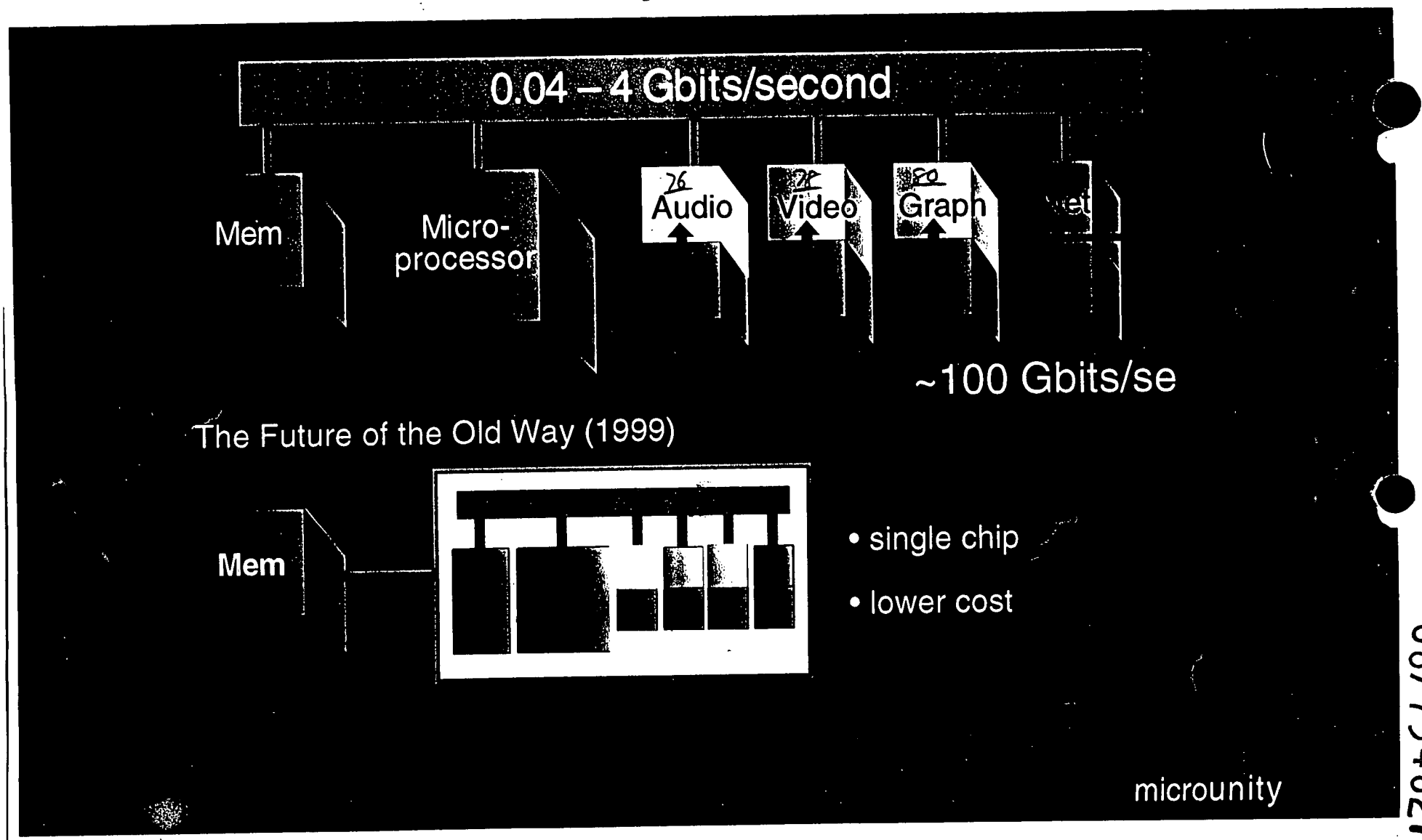
Figure 5



08/754827

Figure 6

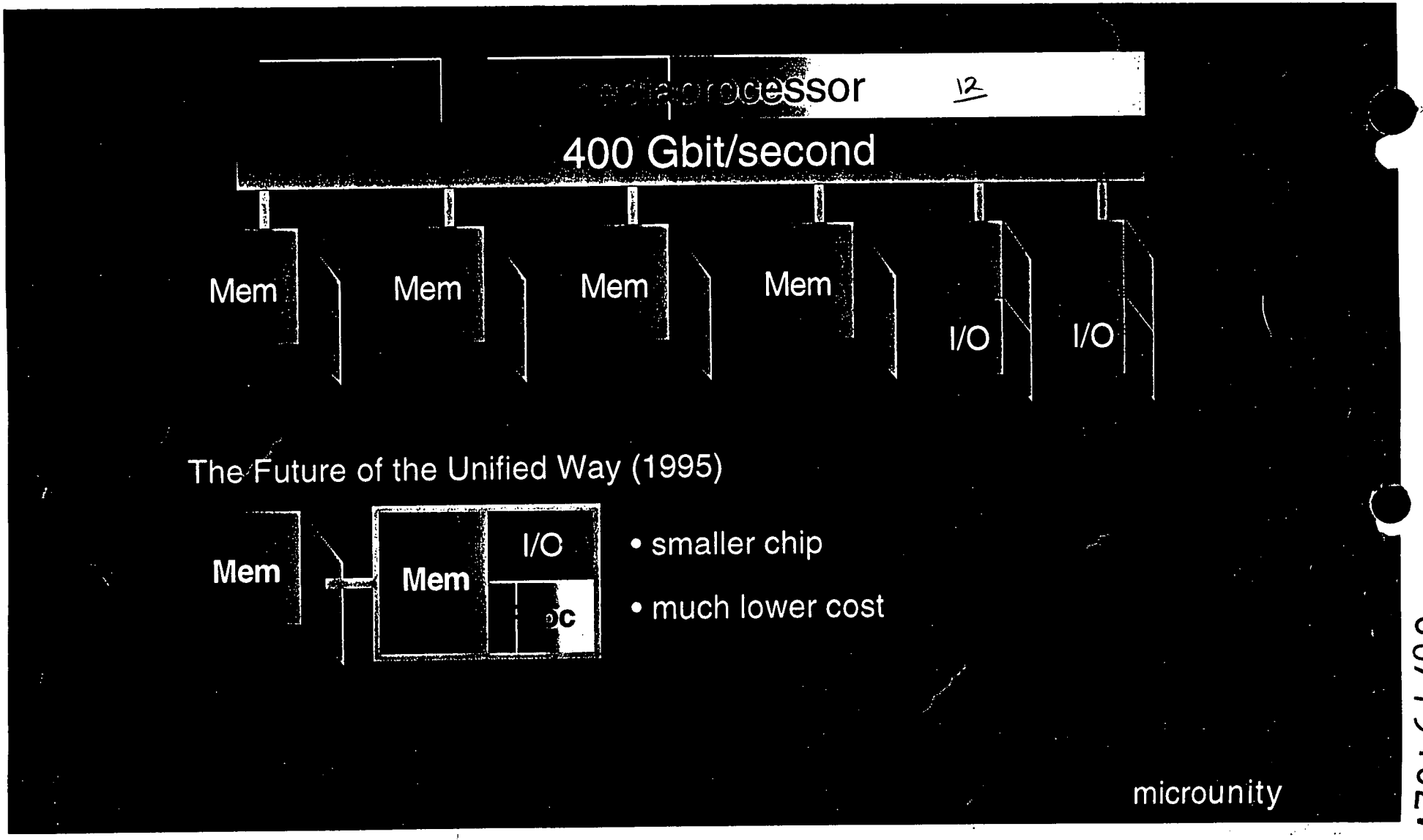


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Figure 7

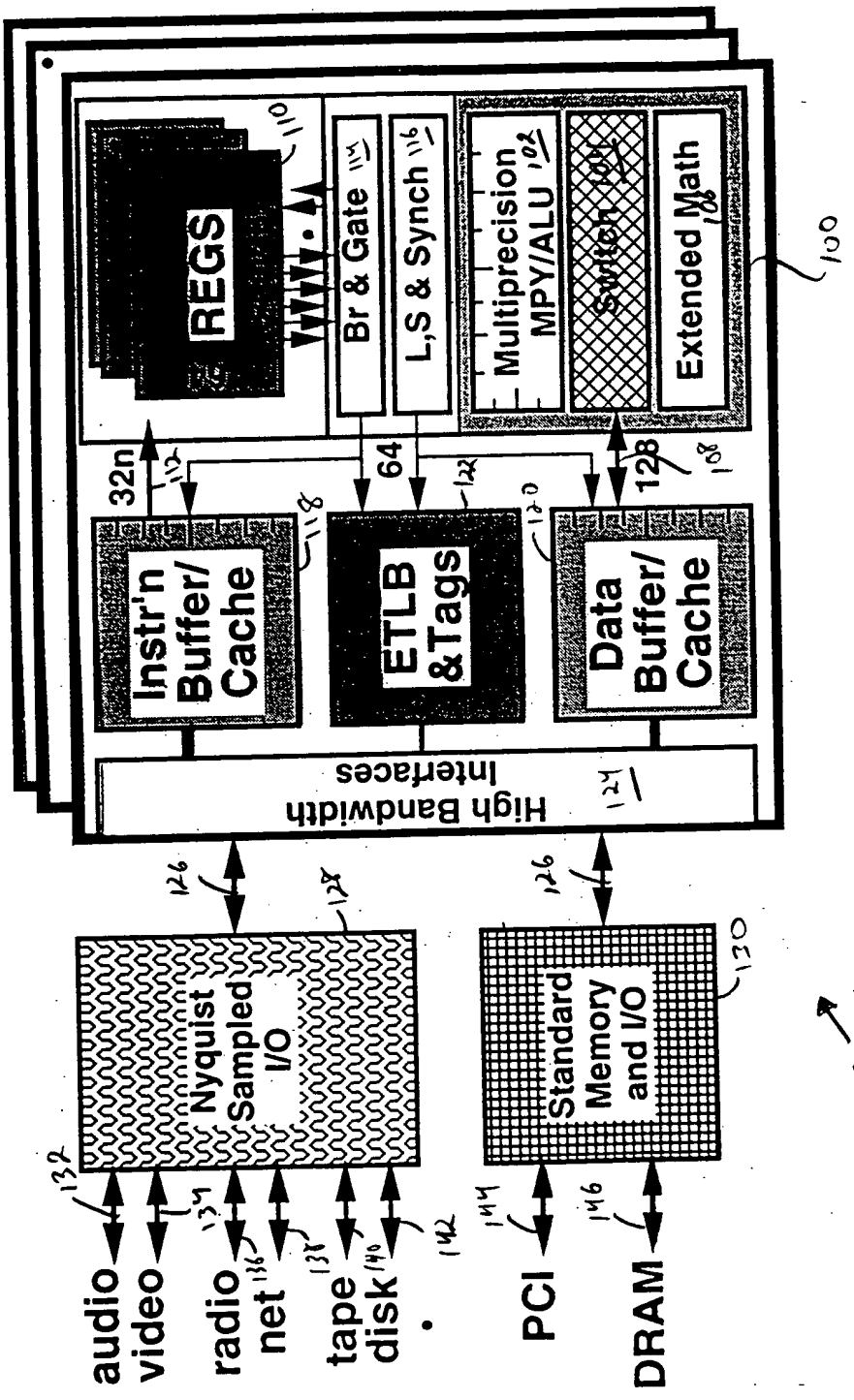
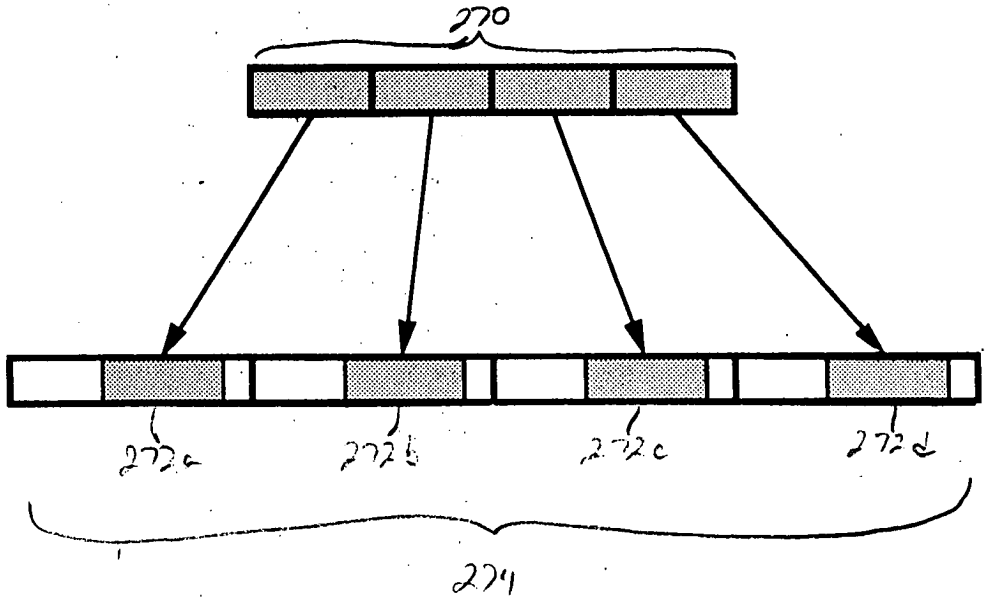

REGS
Br & Gate
L,S & Synch
Multiprecision MPY/ALU
Switch
Extended Math
32n
64
128
Instr'n Buffer/ Cache
ETLB &Tags
Data Buffer/ Cache
High Bandwidth Interfaces
Nyquist Sampled I/O
Standard Memory and I/O
audio
video
radio
net
tape
disk
PCI
DRAM

Figure 8(a)

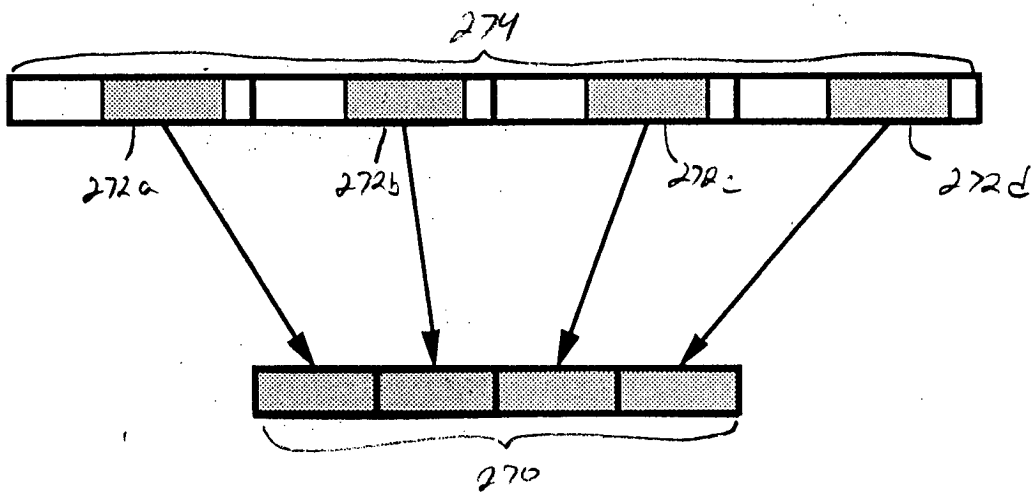
Group Expand



08/754827

Figure 8(b)

Group Compress, Extract

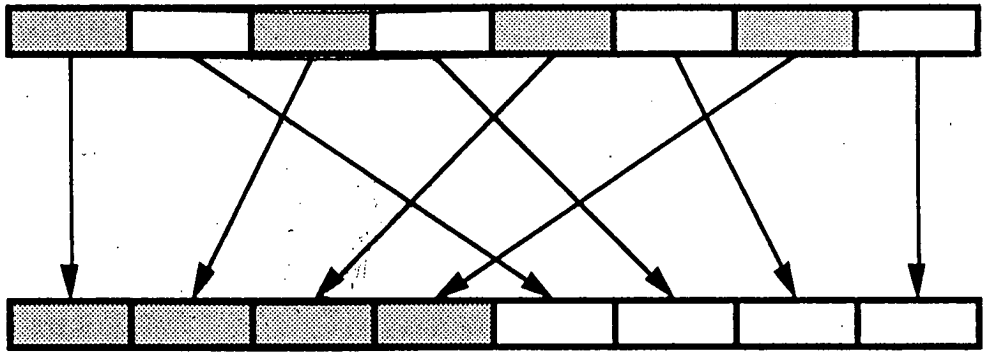


08/754827

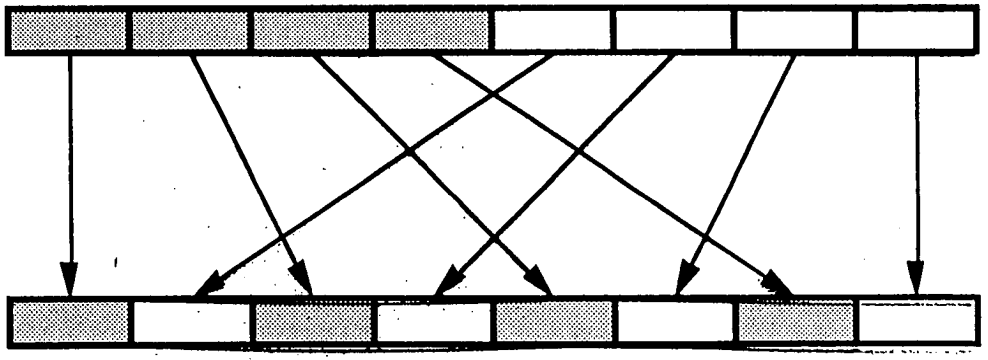
Figure 8(c)

Group Deal, Shuffle

- Group Deal: 128 bits to 128 bits



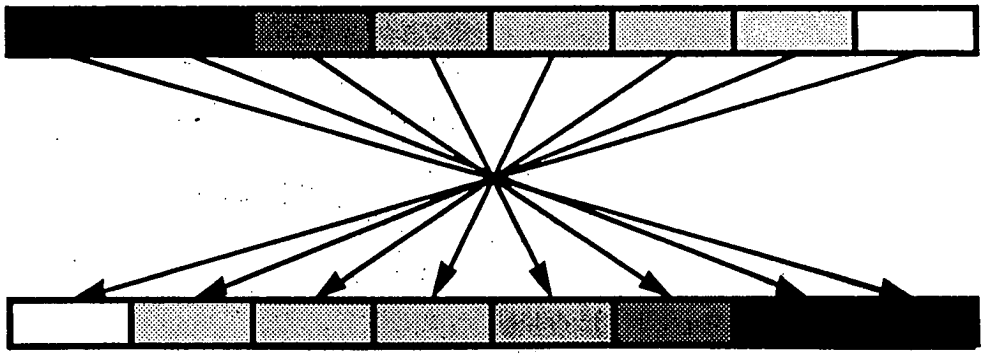
- Group Shuffle: 128 bits to 128 bits



08/754827

Figure 8(d)

Group Swizzle (Copy-Swap)

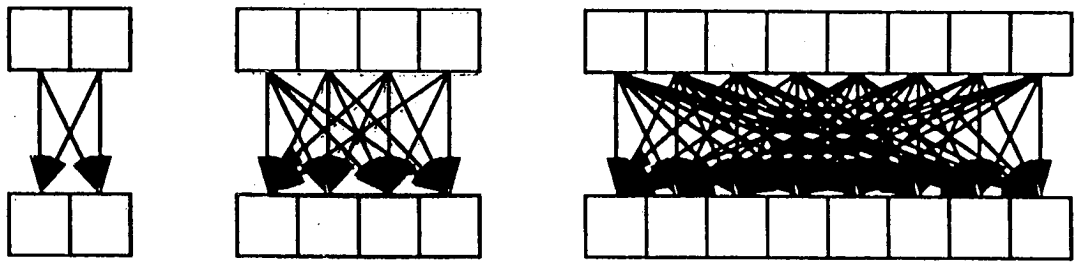


08/754827

Figure 8(e)

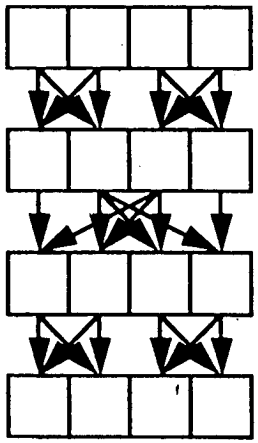
Group Permute

2-mux 4-mux 8-mux

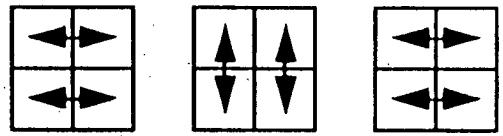


Benes network: multistage permutation

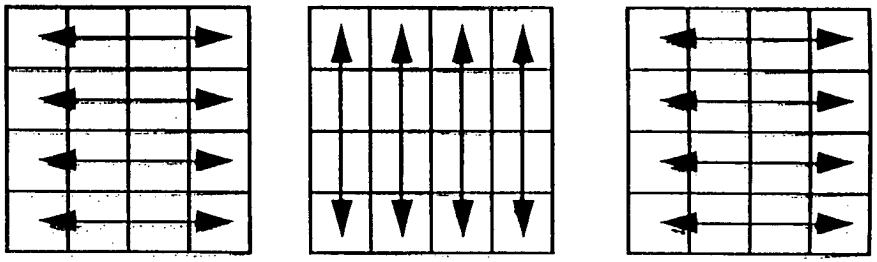
4-mux, 3 stage



4-mux, two-dimensional (3-stage)



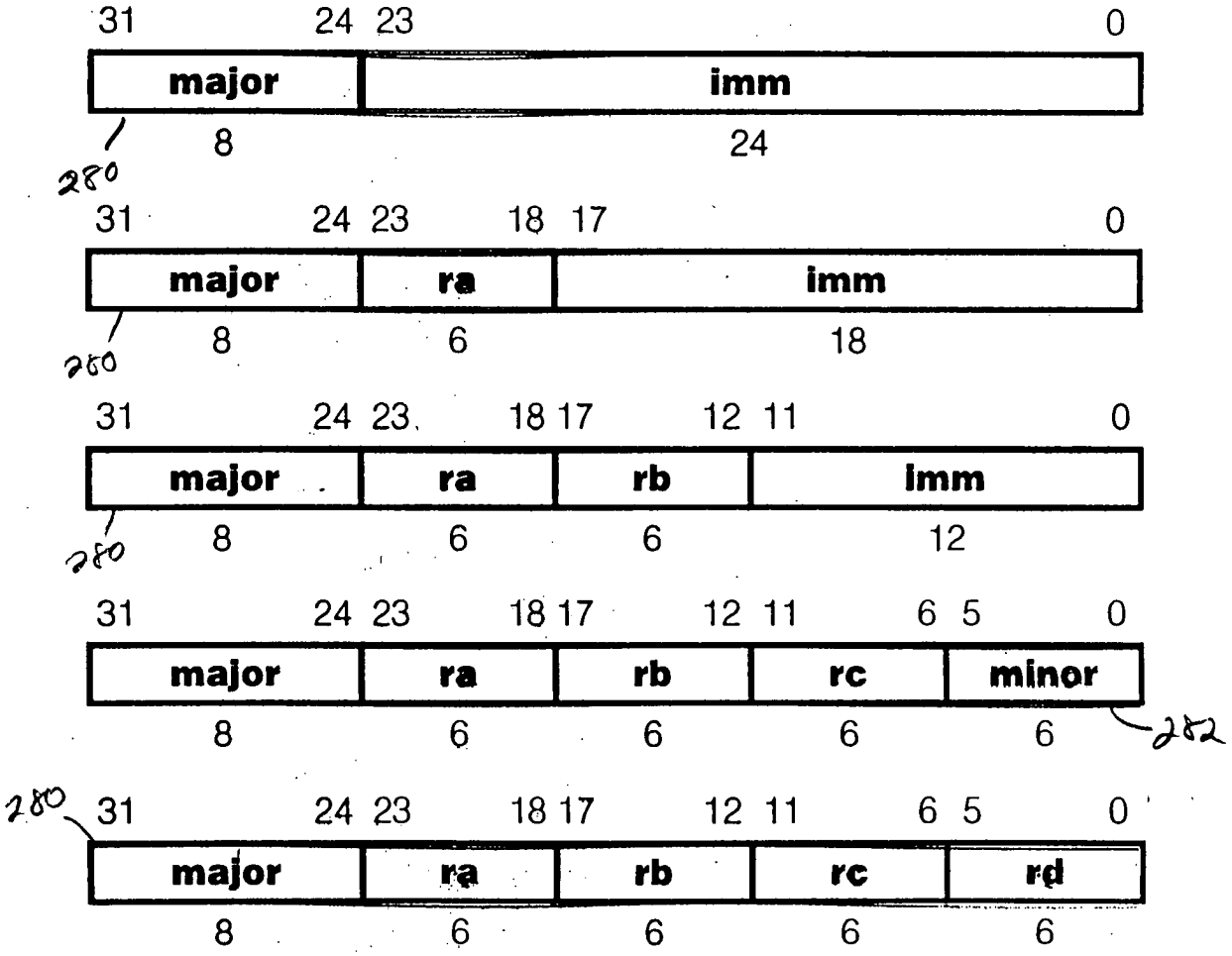
16-mux, two-dimensional (3-stage)



08/754827

Figure 9(a)

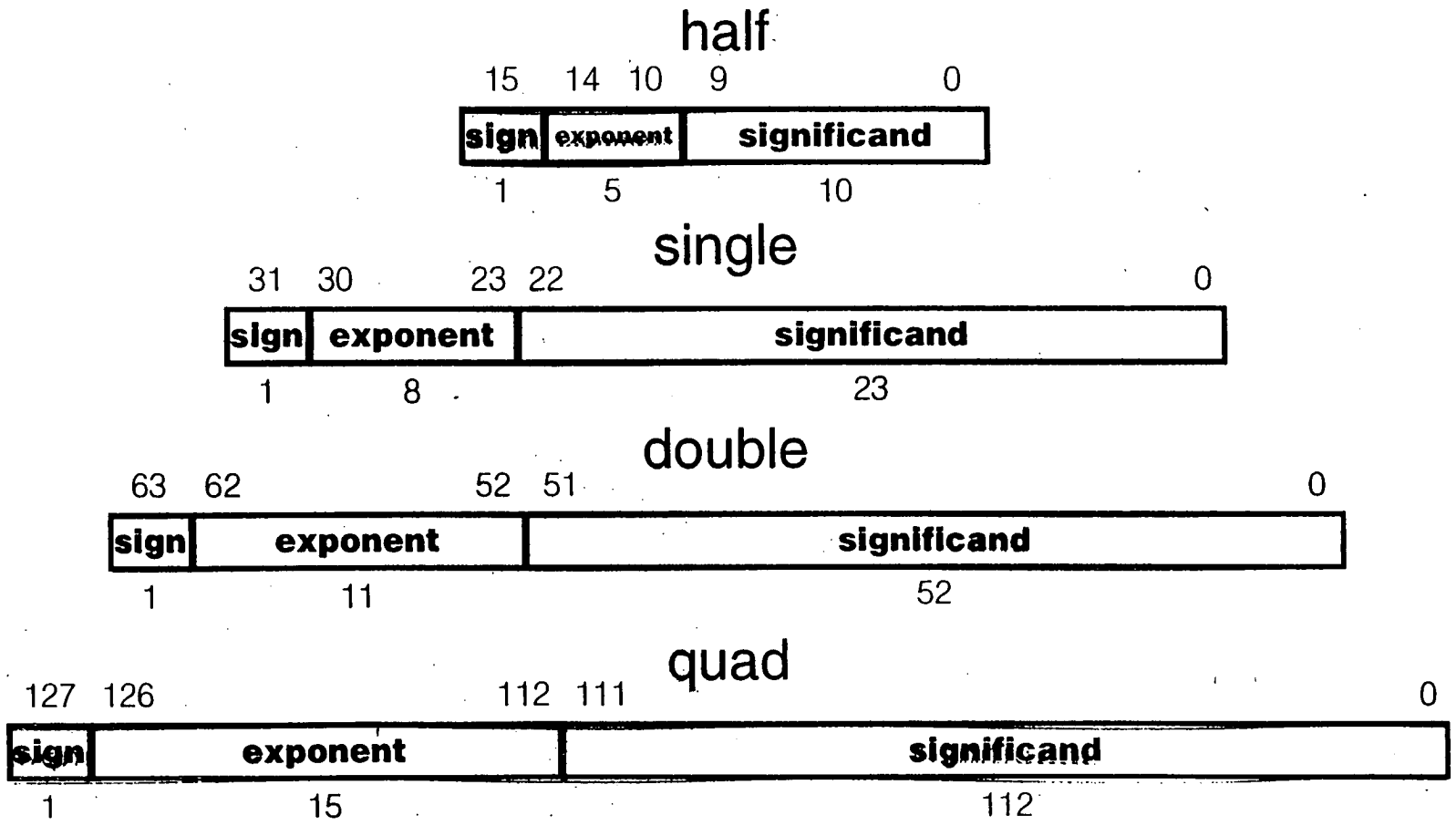
Instruction Formats



08/754827

Figure 9(b)

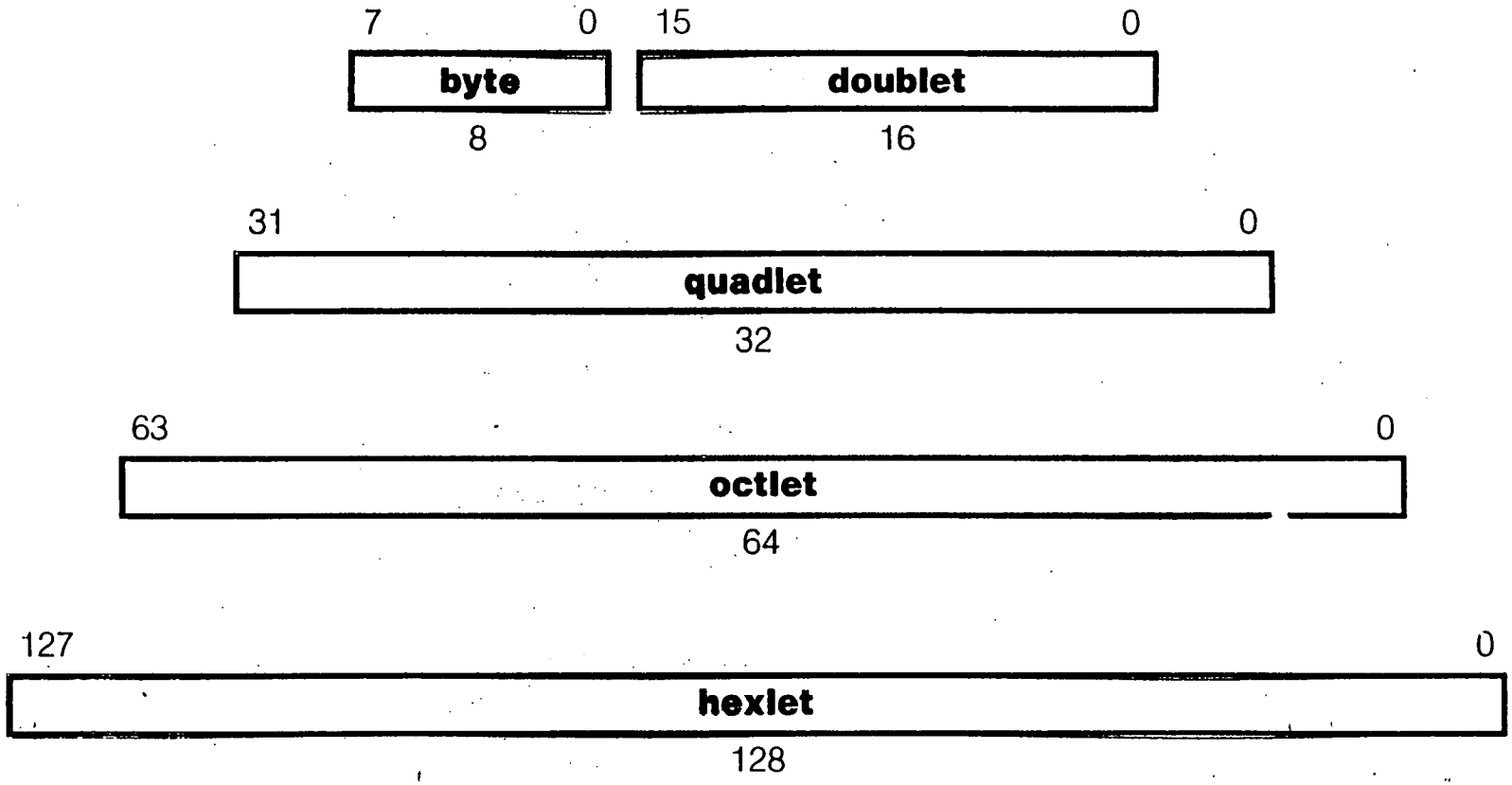
Floating-point Data Sizes



08/754827

Figure 9(c)

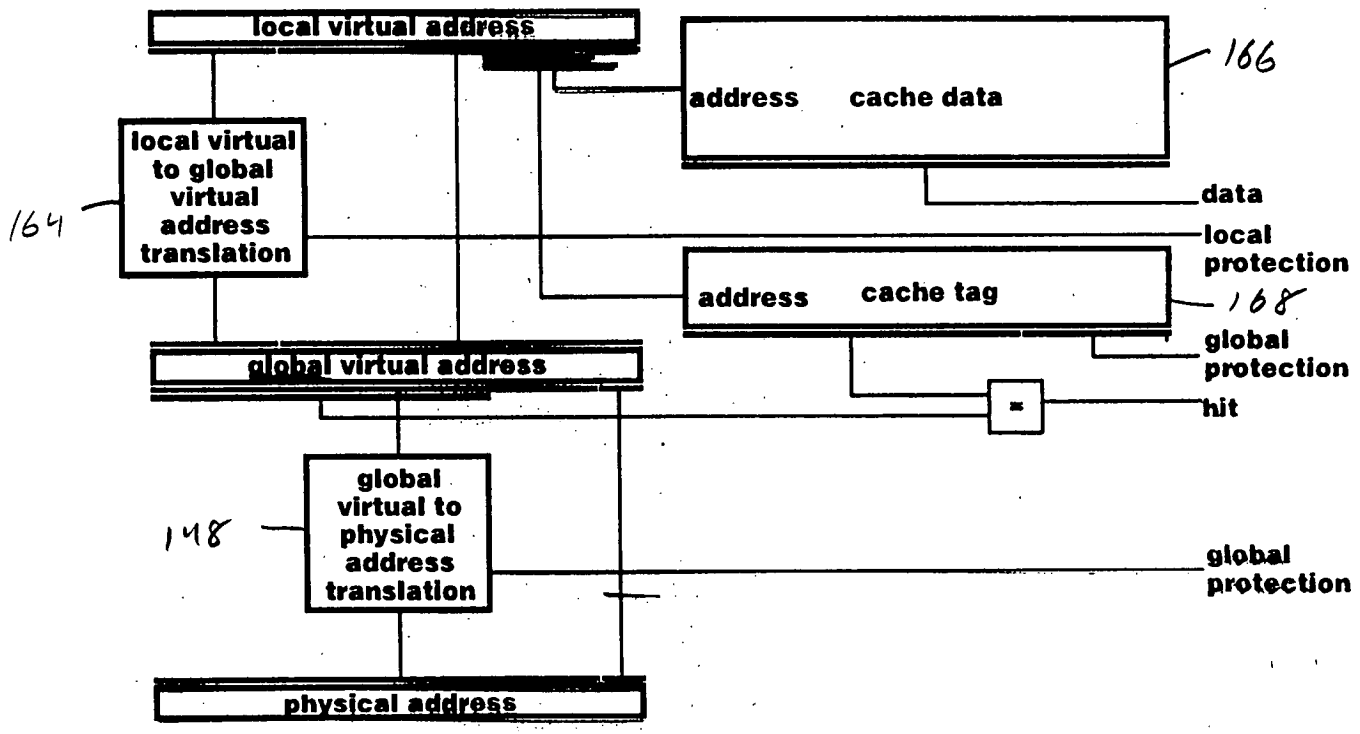
Fixed-Point Data Sizes



08/754827

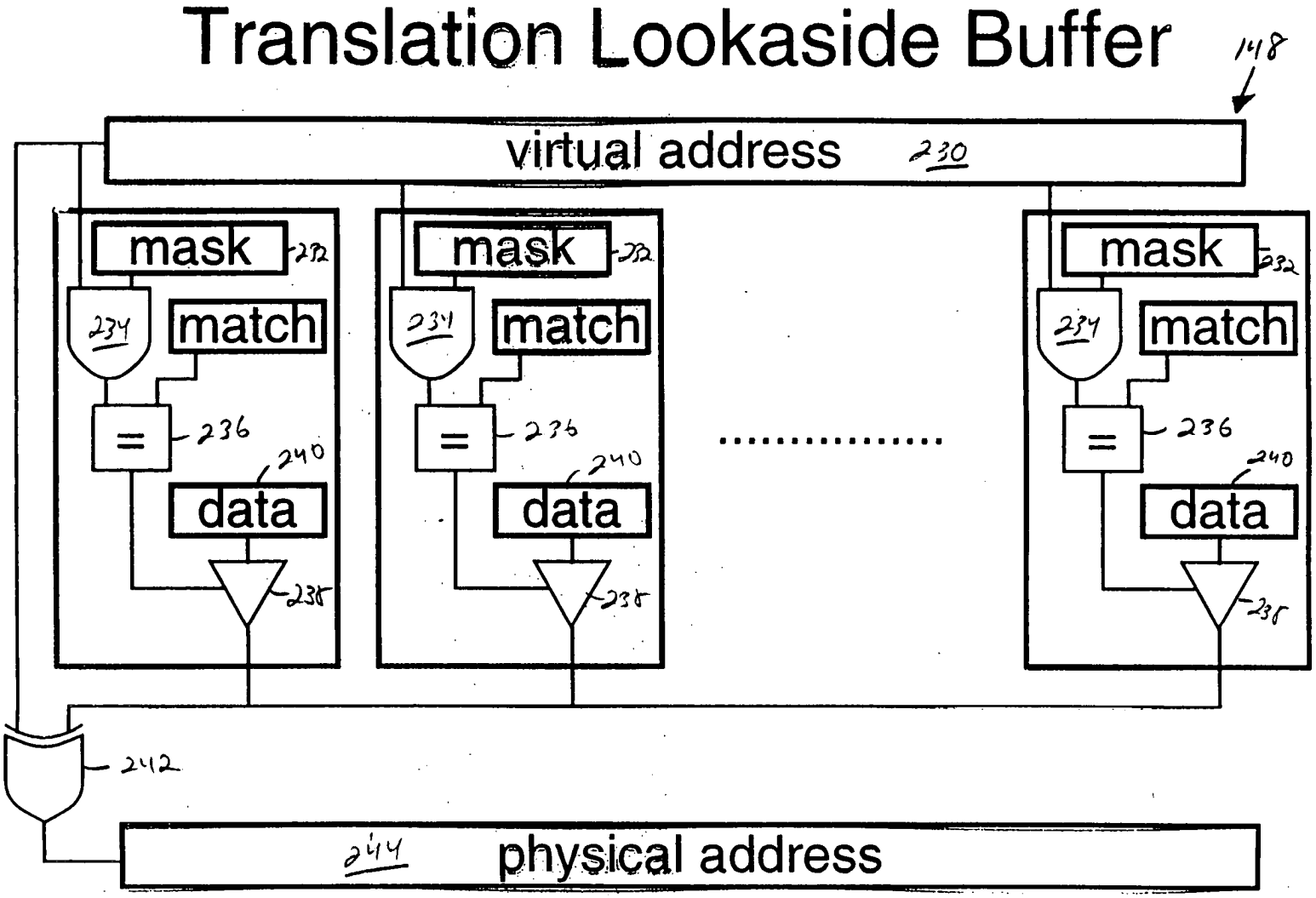
Figure 10(a)

Translation Block Diagram



08/754827

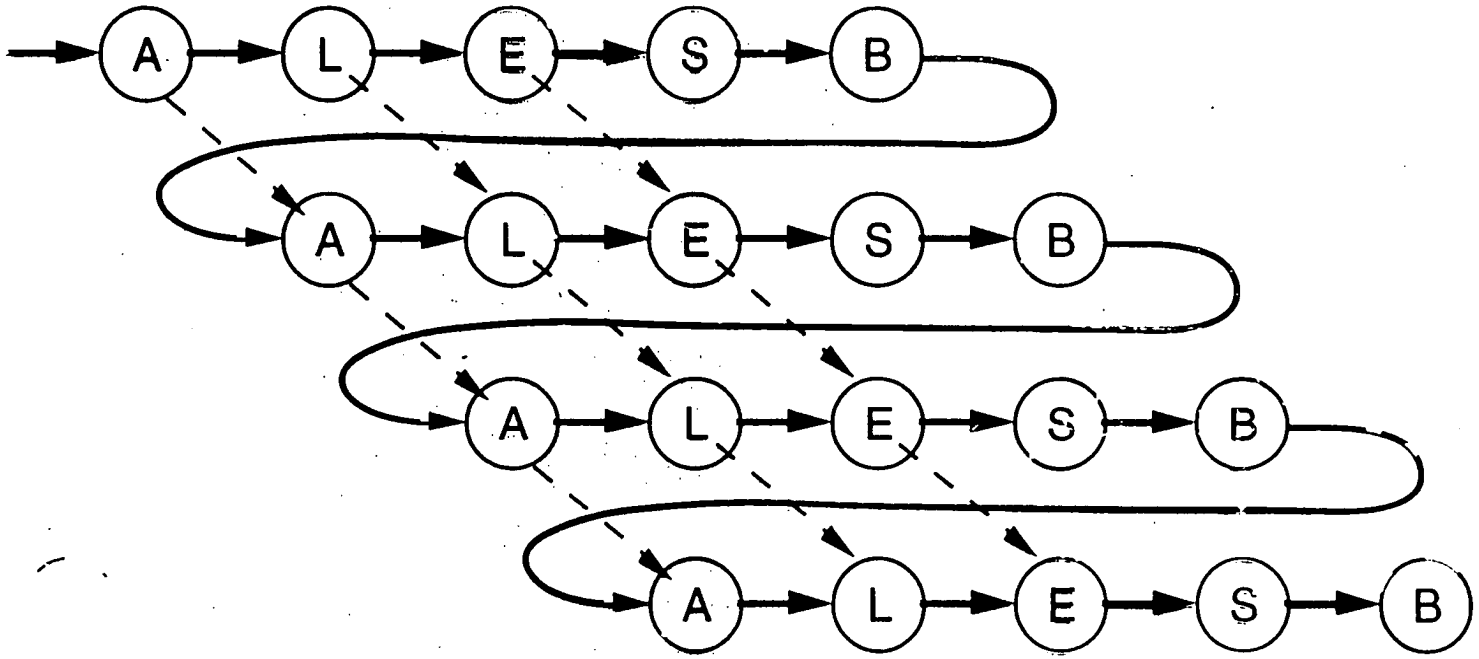
Figure 10(b)



08/754827

Figure 11

Superstring Pipeline



08/754827

Figure 12

Superspring Pipeline

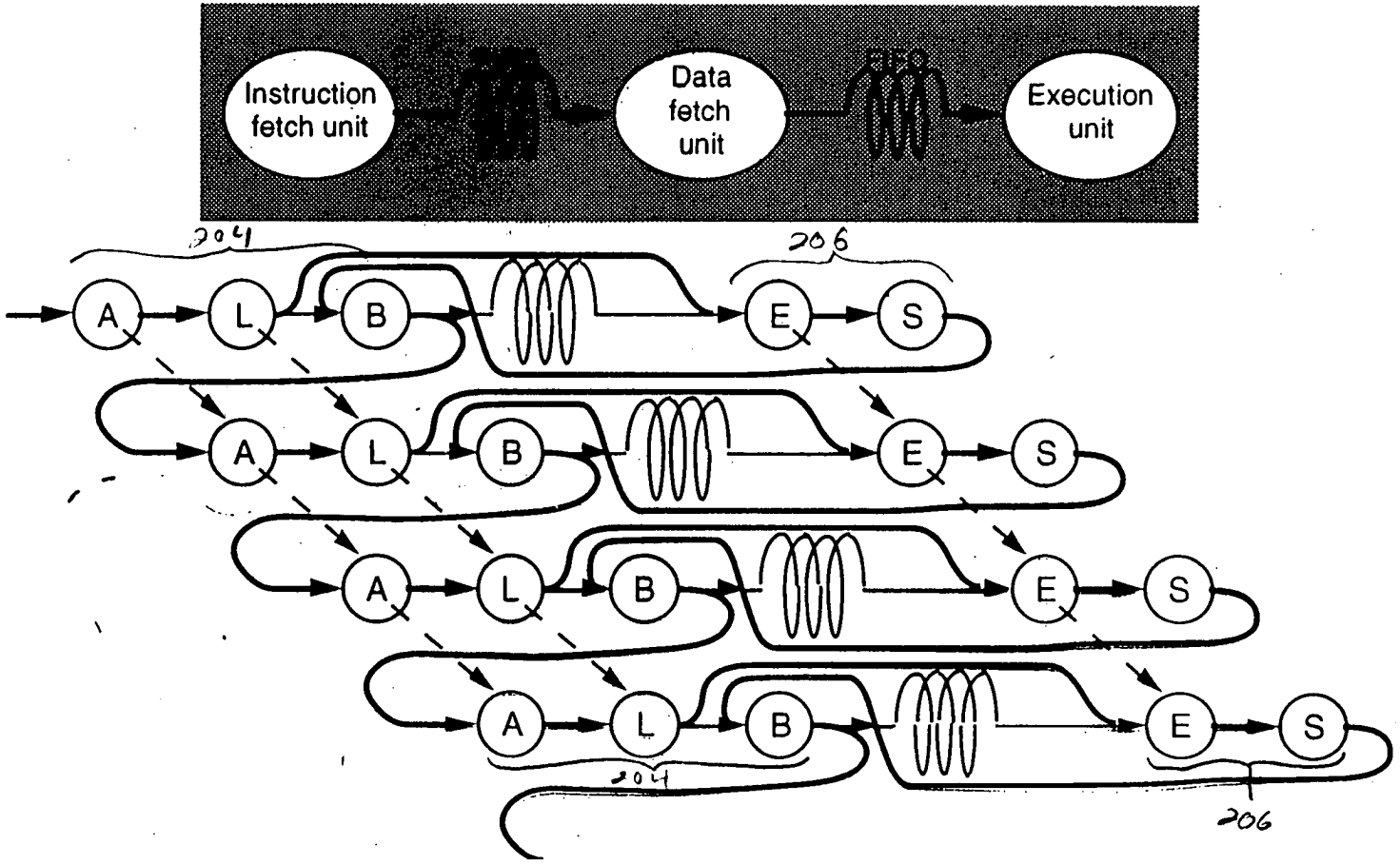


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Figure 13

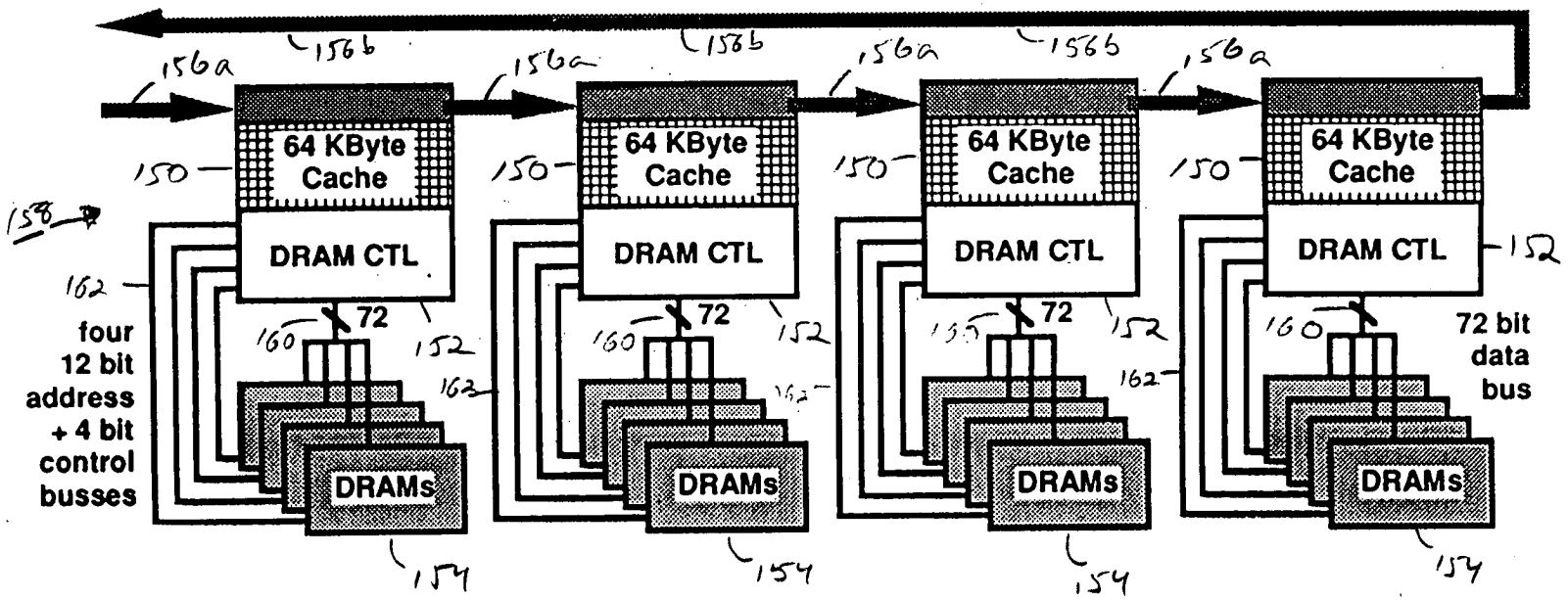

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Figure 14

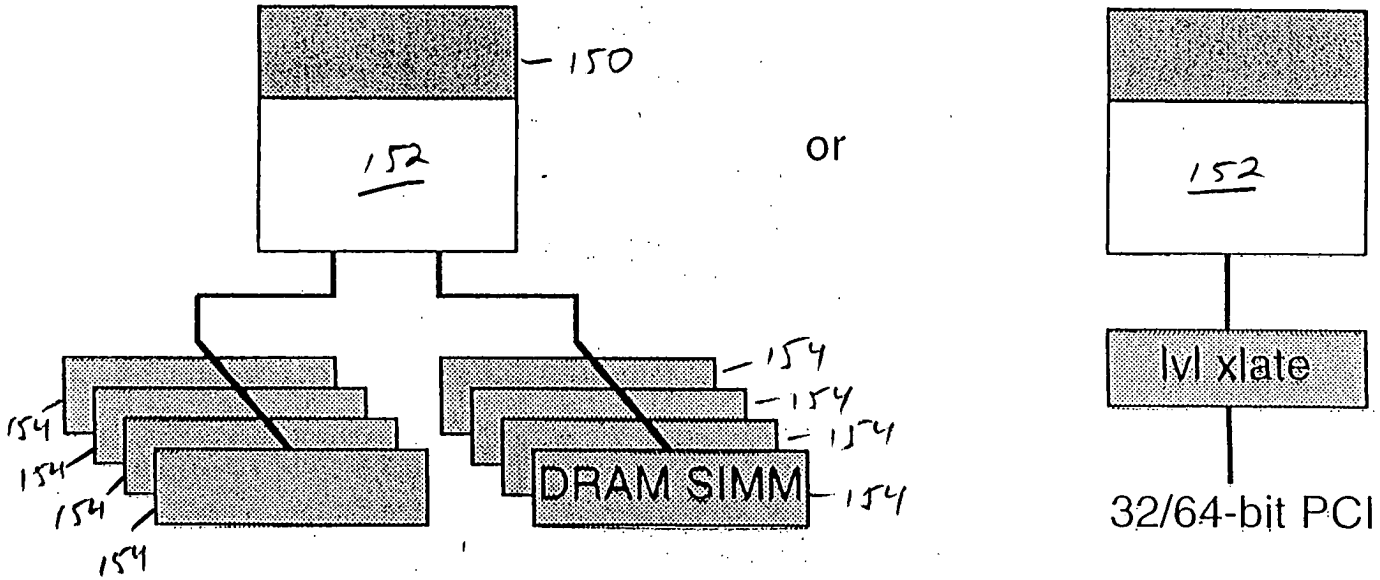

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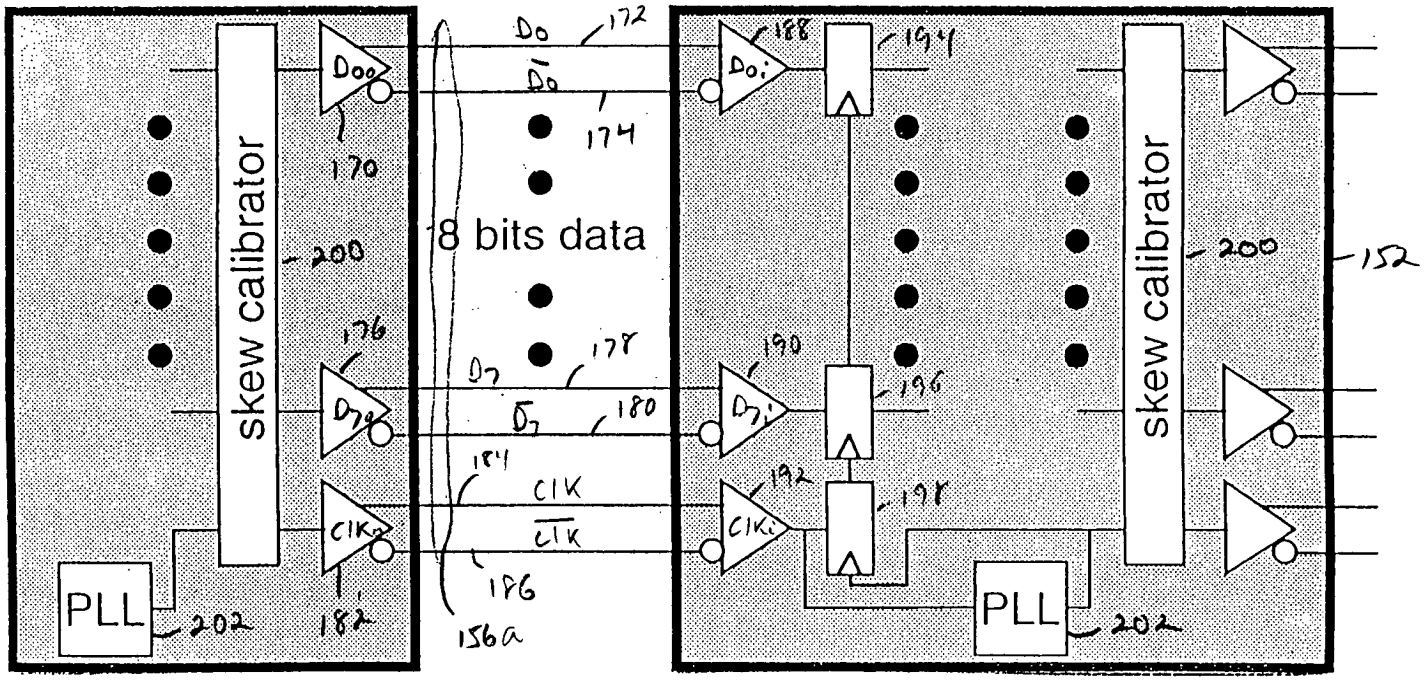
Figure 15



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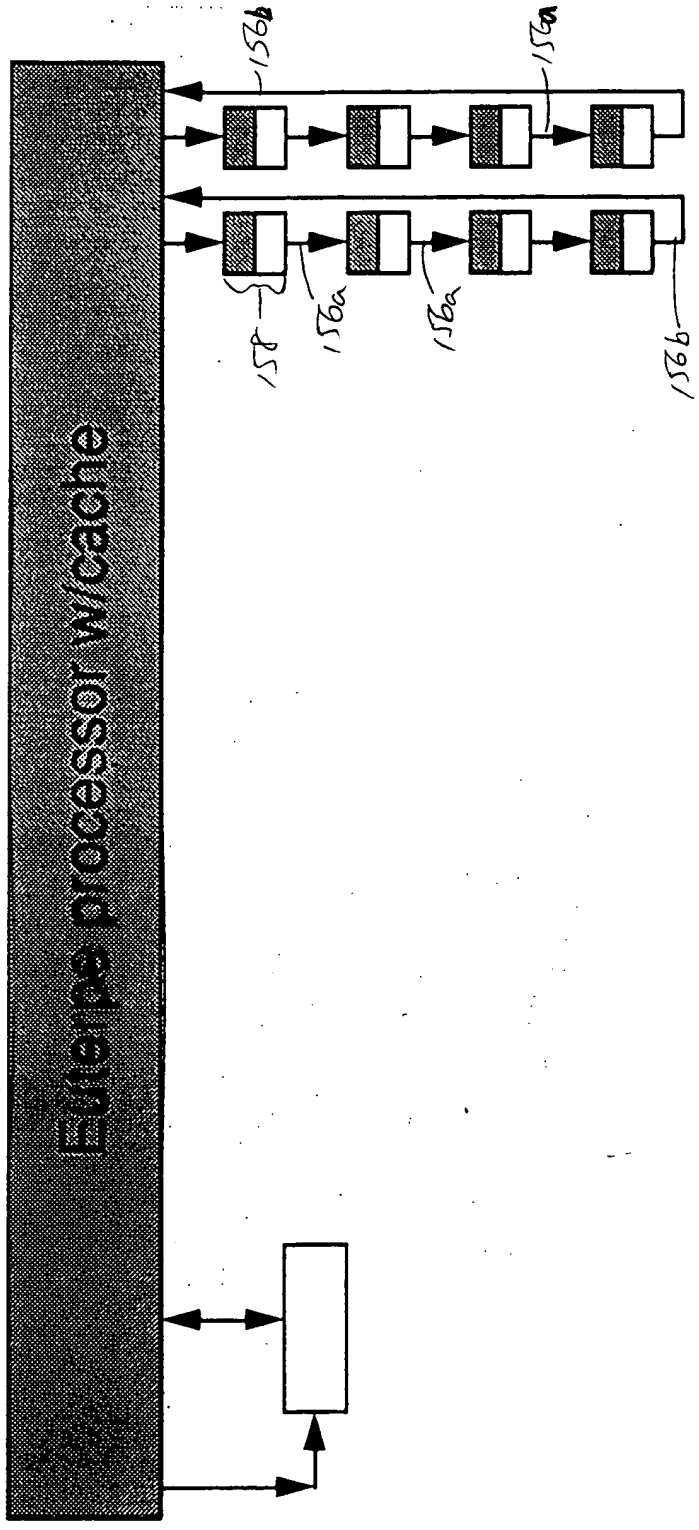

Figure 16(c)

Figure 16(b)

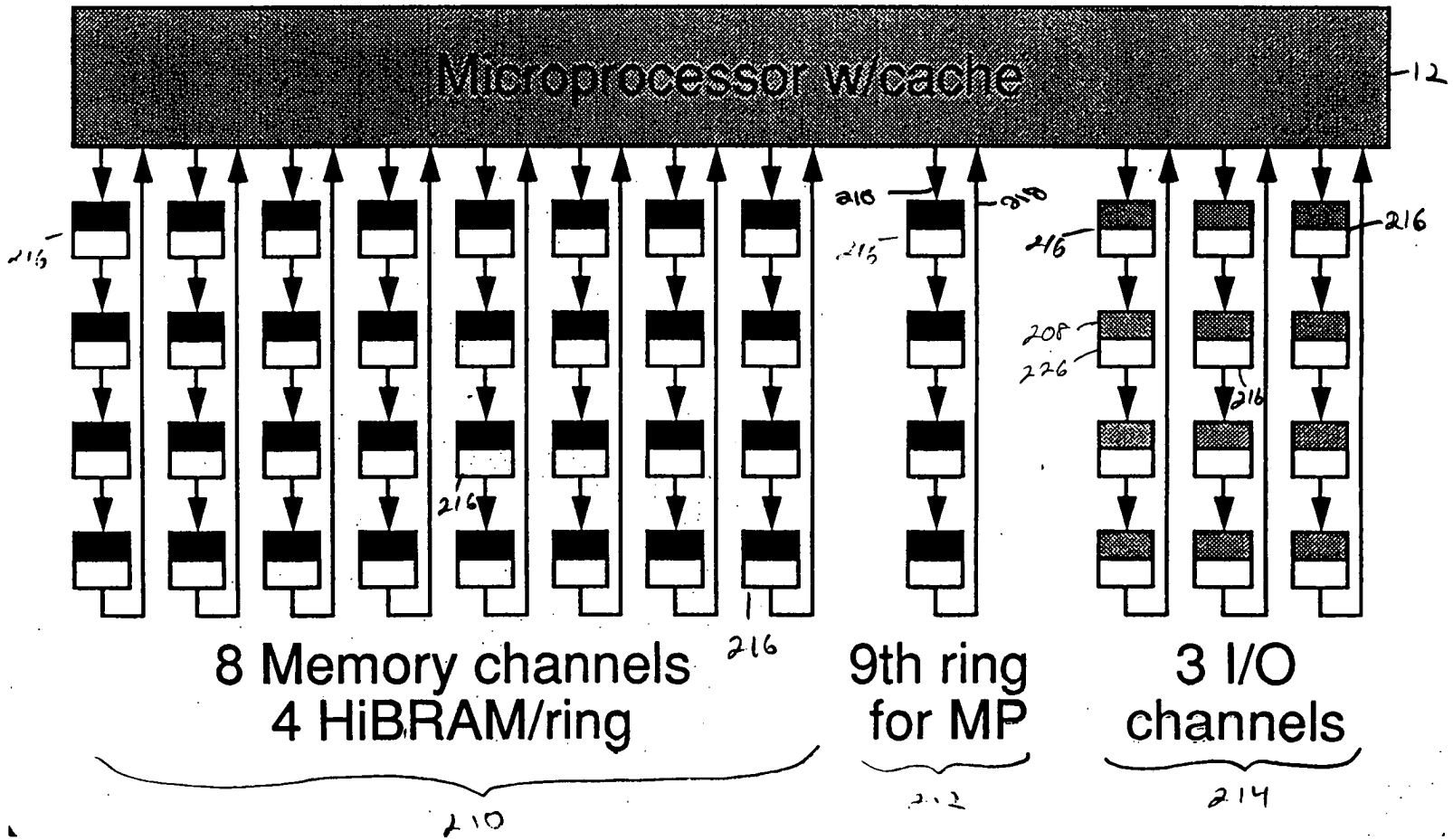

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Figure 17

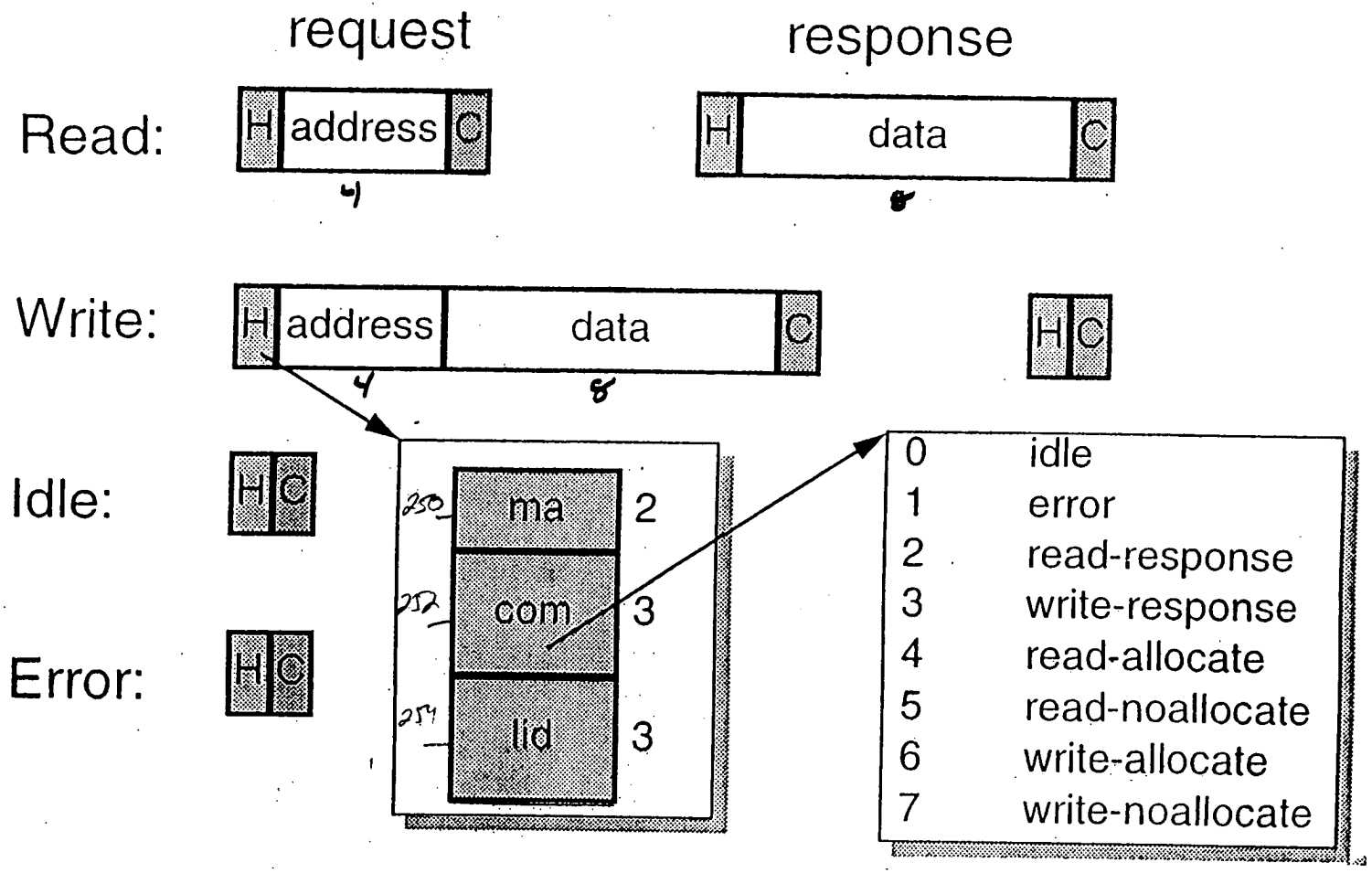

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Figure 18

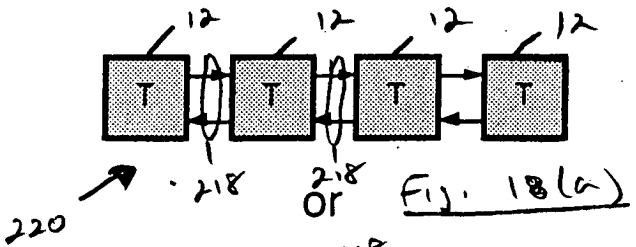


Fig. 18(a)

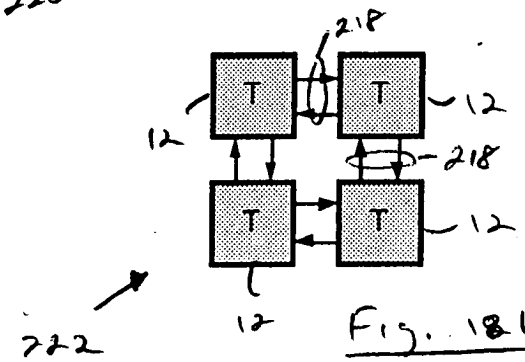


Fig. 18(b)

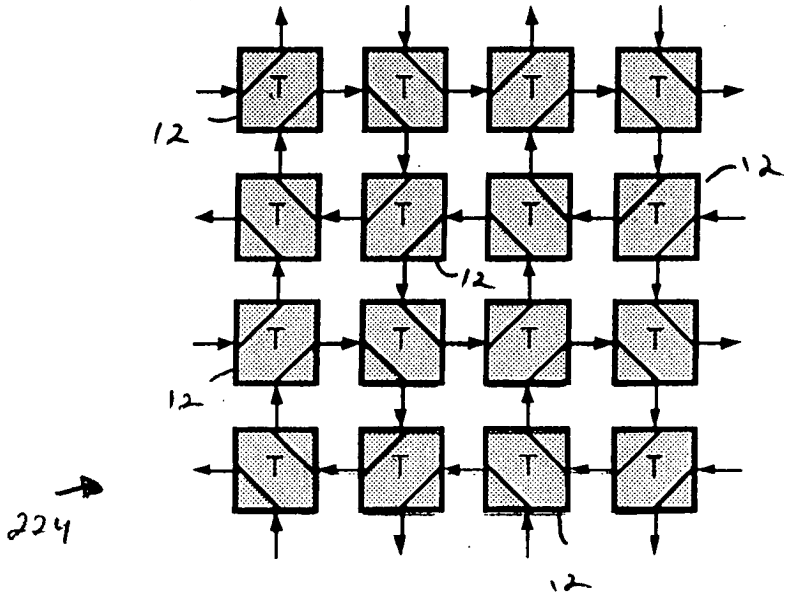
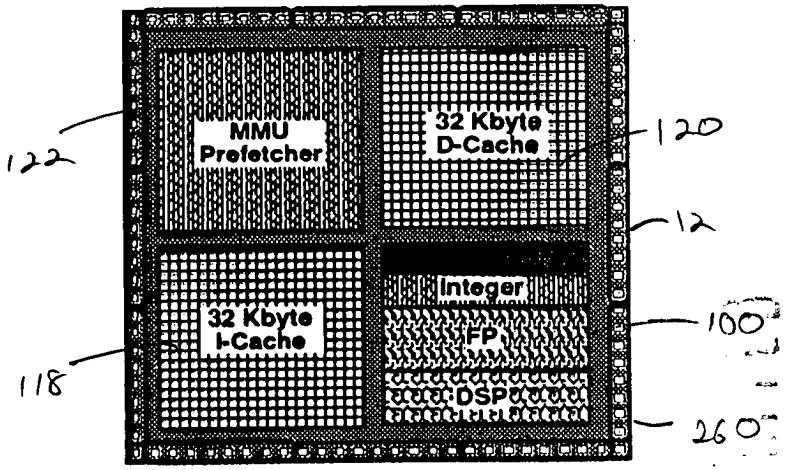


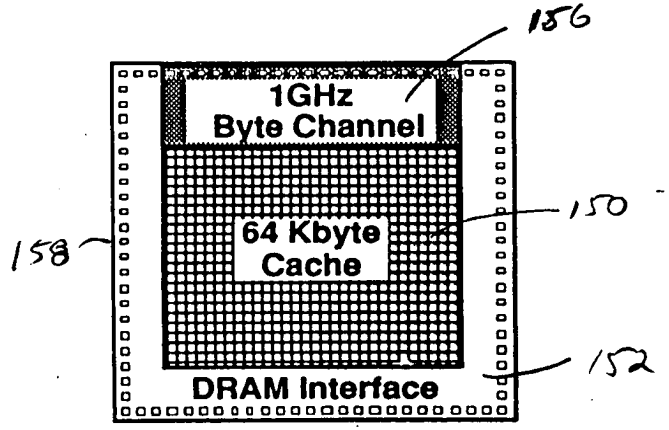
Fig. 18(c)

08/754827

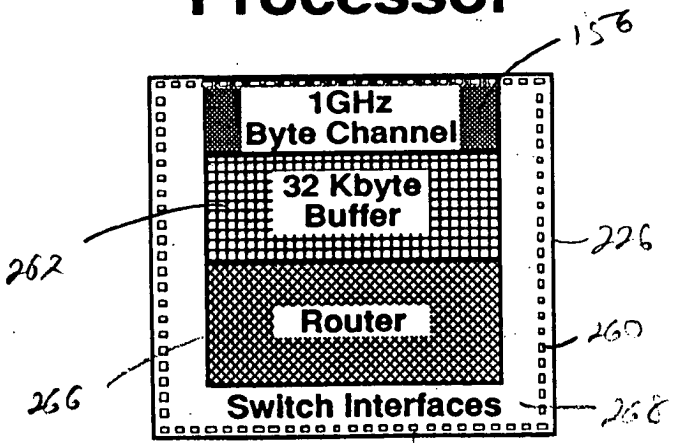
Figure 19



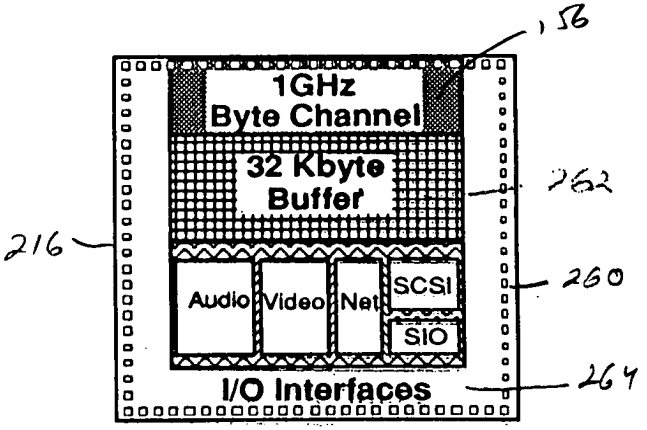
Processor



Memory



Switch



I/O

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